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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/735,555	12/14/2000	Kunihiro Itoh	108075-00022	6570

7590 09/07/2004

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER

CHANG, DANIEL D

ART UNIT	PAPER NUMBER
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2819

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/735,555

Applicant(s)

ITOH ET AL.

Examiner

Daniel D. Chang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 19-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 and 19-37 is/are rejected.
- 7) ☒ Claim(s) 8-11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

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Acknowledgement

Receipt is acknowledged of the Amendment filed October 20, 2003.

Claim Objections

Claim 23 is objected to because of the following informalities: on line 9, "first date circuit" appears to be --first drive circuit--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 19-29, 34, and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (US 4,779,013).

Regarding claims 5, 22, 25, 27, 29, 34, and 37, Tanaka teaches, at least in fig. 8, an output buffer circuit comprising:

a first drive circuit (1), connected to an output terminal (OUT), for receiving an input signal (IN) and generating a first output signal (output of first transistor 5 and second transistor 7) having a first state (logic HIGH/LOW) indicative of one of a high logical level and a low logical level;

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a second drive circuit (3) connected to the output terminal, wherein the second drive circuit generates a second output signal (output of third transistor 17 and fourth transistor 19) having the first state (logic HIGH/LOW); and

a first control circuit (15), connected to the second drive circuit, for generating a first control signal (output of 37 and 39) for driving the second drive circuit on the basis of the input signal (IN) and a delay signal (output of 81) which is generated by adding a predetermined delay (81) to the first output signal such that the second drive circuit generates the second output signal having the first state (HIGH/LOW).

Regarding claims 21, 24, and 26, Tanaka teaches, at least in fig. 8, that the first drive circuit receives an input signal having a sharp waveform (see INPUT POTENTIAL in Fig. 4) and generates the first output signal that has a gentle waveform (see OUTPUT POTENTIAL in Fig. 4; see col. 8, lines 1+; col. 7, lines 37+).

Method claims 1-4, 19-20, 23-24, and 28 are essentially the same in scope as apparatus claims 5, 21, 22, 24-27, 29, 34, and 37 and are rejected similarly.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6, 7, 30-33, 35, and 36, rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Kano (US 5,166,555).

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The teachings of Tanaka have been discussed above.

Regarding claims 6, 30-33, 35, and 36, Tanaka does not disclose that the second drive circuit (third and fourth output transistors) has a lower output impedance than the first drive circuit (first and second output transistors).

Kano discloses that the second drive circuit comprising third and fourth output transistors has wider width channels which means it has a lower output impedance than the first drive circuit for increasing a drivability (see col. 4, lines 50+; col. 6, lines 2+). Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have provided the second drive circuit of Tanaka with the transistors with wider width channel in order to increase the drivability.

Regarding claim 7, Tanaka discloses, that the first control circuit turns on the third output transistor with the first control signal after the first output transistor is turned on by the input signal, and the first control circuit turns on the fourth output transistor with the first control signal after the second output transistor is turned on by the input signal (col. 8, lines 1+; col. 7, 37+).

Response to Arguments

Applicant's arguments with respect to claims 1-11 and 19-37 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

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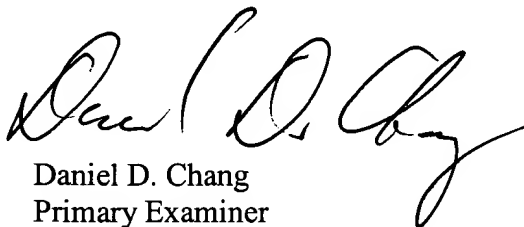
Claims 8-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang
Primary Examiner
Art Unit 2819

DC

**DANIEL CHANG
PRIMARY EXAMINER**